120 03-26-04 AF/2815

Attorney's Docket No. 64.610-062 (YOR920010633US1)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ricky Amos
Serial No.: 09/ 995,031
Filed: Nov. 29, 2001
For: High Temperature Processing Compatible Metal Gate Electrode for FETs and Method for Fabrication

Group Art Unit: 2815
Examiner: Matthew Landau

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF *REVISED* APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the **REVISED** APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on April 22, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING **REVISED** APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
____ small entity $160.00
____ other than a small entity $320.00
x was already paid

Appeal Brief fee due: $ 0

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 305 399 680 US in an envelope addressed to Box: Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Kathy Dixon

Dated: Mar. 25/04

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 400.00	$200.00
☐	three months	$ 920.00	$460.00
☐	four months	$1,440.00	$720.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

__X__ was already paid
Appeal Brief Fee: $__0__
Extension fee (if any) $_____

TOTAL FEE DUE: $____0____

6. FEE PAYMENT

____ Attached is a check in the sum of $ __0__
__X__ Charge Deposit Account No. 50-0510 any fees which may be required, a duplicate of this transmittal is attached.

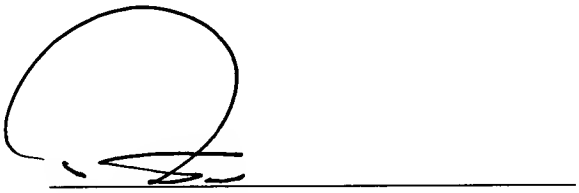
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. __50-0510__.

And/Or

__X__ If any additional fee for claims is required, please charge Account No. __50-0510__.



Signature of Attorney

Registration No. 31,311

Randy W. Tung

Telephone: (248) 540-4040

Tung & Associates
838 W. Long Lake Road, Ste. 120
Bloomfield Hills, Michigan 48302

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Ricky Amos

Group Art Unit: 2815
Examiner: Matthew Landau

Serial No.: 09/995,031

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Attorney Docket No.: YOR920010633US1 (062)

EXPRESS MAIL CERTIFICATE

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I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Kathy Dixon

***REVISED* APPEAL BRIEF**

Mail Stop: Appeal
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants appeal in the captioned application from the Examiner's final rejection, dated January 22, 2003, of claims 1-16 under 35 USC §102(e) as being anticipated by Maria et al '995 publication and Inumiya et al '997.

It is urged that the rejection be reversed and that all the claims be allowed.

(1) **REAL PARTY IN INTEREST**

The real party in interest in the present appeal is the recorded Assignee of International Business Machines Corporation.

(2) **RELATED APPEALS AND INTERFERENCES**

There are no other appeals or interferences that are known to the Appellants, the Appellants' legal representative, or the assignee.

(3) **STATUS OF CLAIMS**

Claims 1-16 are pending in the application.

Claims 1-16 stand rejected.

(4) **STATUS OF AMENDMENTS**

A Request for Reconsideration was filed on or about March 24, 2003 which contains claim amendments to claims 1 and 10.

An Advisory Action was mailed April 3, 2003 by the Examiner rejecting the entering of claim amendments in the Request for Reconsideration.

A Notice of Appeal was filed on or about April 22, 2003.

(5) SUMMARY OF THE INVENTION

001 The invention relates to a metal gate electrode that is compatible with high temperature processing of p-type FETs.

(Specification, paragraph 001)

0013 In a preferred embodiment, a metal oxide semiconductor device is provided which includes a semi-conducting substrate that has source and drain regions; a gate dielectric layer of less than 100 Å thickness on the semi-conducting substrate; and a gate formed of a metal selected from the group consisting of Re, Rh, Ir, Pt and Ru on top of the gate dielectric layer.

0014 In the metal oxide semiconductor device, the gate dielectric layer may have a thickness preferably less than 50 Å. The gate dielectric layer may be formed of a material selected from SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof, or may be formed of a material selected from Al_2O_3, HfO_2, ZrO_2, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions. In one specific embodiment, the dielectric layer may be formed of SiO_2, while the semi-conducting substrate may be formed of silicon. The semi-conducting substrate may be p-type or n-type. The semi-

conducting substrate may be formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

0015 The present invention is further directed to a field effect transistor that includes a semi-conducting substrate that has at least one source and one drain region; a gate dielectric layer of less than 100 Å thickness on the semi-conducting substrate; and a gate formed of a metal selected from the group consisting of Re, Rh, Ir, Pt and Ru on top of the gate dielectric layer.

0016 In the field effect transistor, the gate dielectric layer may have a thickness preferably less than 50 Å, and may be formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof. The dielectric material layer may further be formed of a material selected from Al_2O_3, HfO_2, ZrO_2, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions. The semi-conducting substrate may be p-type or n-type, or may be formed of a material selected from silicon, SiGe, SOI and GaAs. In one specific embodiment, the

semi-conducting substrate of the FET is formed of silicon while the gate dielectric layer is formed of SiO_2.

(Specification, paragraphs 0013-0016)

(6) ISSUE

Issue I

Is the rejection of claims 1-4 and 6-15 under 35 USC §102(e) as being anticipated by Maria et al proper when such reference does not teach or suggest the specifically claimed limitations in the present application?

Issue II

Is the rejection of claims 1, 5, 10 and 16 under 35 USC §102(e) over Inumiya et al '997 proper when such reference does not teach or suggest the specifically claimed limitations in the present application?

(7) GROUPING OF CLAIMS

The rejection of claims 1-4 and 6-15 are contested as a group.

The rejection of claims 1, 5, 10 and 16 are contested as a separate group.

(8) **ARGUMENTS**

A petition to the Commissioner to enter the claim amendments made in the Request for Reconsideration dated 03/24/2003 is being filed simultaneously with this Appeal Brief. The petition argues that the refusal of entering the claim amendments by the Examiner in the Advisory Action mailed 04/03/2003 is improper and must be reversed. The arguments presented in this brief therefore assumes that such petition is granted by the Commissioner and that the claim amendments contained in the Request for Reconsideration have been entered.

ISSUE I

Claims 1-4 and 6-15 are rejected under 35 USC §102(e) as being anticipated by Maria et al.

Dependent claims 1 and 10 have been amended to more narrowly recite a gate formed of a metal that is **Re** or **Rh**. The Appellants respectfully submit that such gate materials are not taught or disclosed by Maria et al. Instead, Maria et al discloses a gate electrode materials at page 4, paragraph 0036 as:

> "Alternatively, the gate electrodes 22a, 22b may comprise identical materials such as **TaN, Pt, Ru, RuO, Ir, IrO_2 and/or $Ta_{1-x}N_y$.**"

The Appellants respectfully submit that the newly amended independent claims 1, 10, and their dependent claims 2-4, 6-9 and 11-15, are therefore not anticipated by Maria et al. The final rejection of these claims is improper and must be reversed.

ISSUE II

Claims 1, 5, 10 and 16 are rejected under 35 USC §102(e) as being anticipated by Inumiya et al '997.

Inumiya et al discloses at col. 10, lines 65+:

> "Further, a gate electrode 20 consisting of a conductive film (such as a **TiN** film, a **Ru** film, a **W** film, a **Cu** film or a laminate including any of these films such as **W/TiN**) and having its bottom surrounded by the gate insulating film ..."

Inumiya et al therefore does not teach or disclose the gate metal of **Re** and **Rh** as now recited in the newly amended independent claims 1 and 10.

The rejection of claims 1, 5, 10 and 16 under 35 USC §102(e) based on Inumiya et al is improper and must be reversed.

CLOSING

In summary, the Appellants have shown that their claimed invention is fully supported by a body of evidence of non-anticipation. It is therefore respectfully submitted that such evidence of non-anticipation overcomes any showing of anticipation presented by the Examiner. The Appellants therefore submit that the final rejection of their claims 1-16 is improper under 35 USC §102(e).

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

Randy W. Tung
Registration No. 31,311
Telephone: (248) 540-4040

RWT\kd

CLAIM APPENDIX

1. A metal oxide semiconductor (MOS) device comprising:

a semi-conducting substrate having source and drain regions;

a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate; and

a gate formed of a metal selected from the group consisting of Re, Rh, Ir and Ru on top of said gate dielectric layer.

2. A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer having a thickness of less than 50 Å.

3. A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

4. A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is formed of a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

5. A metal oxide semiconductor device according to claim 1, wherein said dielectric layer is formed of SiO_2.

6. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate has at least one source and one drain region.

7. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is p-type or n-type.

8. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

9. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of silicon.

10. A field effect transistor (FET)comprising:

a semi-conducting substrate having at least one source and one drain region;

a gate dielectric layer of less than 100 Å thickness on the semi-conducting substrate; and

a gate formed of a metal selected from the group consisting of Re, Rh, Ir and Ru on top of the gate dielectric layer.

11. A field effect transistor according to claim 10, wherein the gate dielectric layer has a thickness of less than 50 Å.

12. A field effect transistor according to claim 10, wherein said gate dielectric layer is formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

13. A field effect transistor according to claim 10, wherein said gate dielectric layer is formed of a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

14. A field effect transistor according to claim 10, wherein said semi-conducting substrate is p-type or n-type.

15. A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

16. A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of silicon and said gate dielectric layer is SiO_2.